CAMDEN S. LARSON

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CAREER OBJECTIVE

Dedicated and results-driven computer engineering student with a passion for software/hardware design and the development of AI/ML models. Strong collaborator with excellent written and oral presentation skills, coupled with a competitive and hardworking nature. Ability to balance numerous responsibilities simultaneously. Eager to contribute to innovative projects that combine my hardware and AI interests.

NOTABLE SKILLS AND CERTIFICATIONS

-PYTHON	-VERILOG/SYSTEMVERILOG	-JAVA	-CLOUD PRACTITIONER (AWS)
-VHDL	-DIGITAL LOGIC DESIGN	-GIT	-CIRCUIT SIMULATION (SPICE)

EXPERIENCE

Data Science & Analytics Intern May 2024 – August 2025

DULLES, VA – NIGHTWING (2024 DIVESTITURE FROM RAYTHEON)

- Deployed data products and automated workflows for cross-functional stakeholders using Python, Tableau, and Power Automate as part of a data mesh and enterprise AI transformation initiative.
- Designed and implemented ETL-driven analytics products incorporating AI/ML models, advanced visualization, and reusable cloud infrastructure improvements through Terraform refactoring.
- Built and deployed a Windows system tray acronym disambiguation assistant using Retrieval Augmented Generation (RAG) with Chroma DB, SQLite, and LLM ranking, enabling context-aware tooltip lookups, hotkeys, and sharing of acronym dictionaries. Presented results to technical and non-technical leadership.

VTOL (Vertical Take-Off and Landing) Club Fall 2024 – Present

- Vertical Flight Society Design-Build-Vertical-Flight Competition Electronics/Software team member.
- Developed a comprehensive python-based drone control toolkit that leveraged MAVLink and Dronekit protocols to enable autonomous flight mission planning and execution for VTOL unmanned aerial vehicles. Implemented core navigation utilities as well as failsafe mode/arming management.
- Created mission simulation infrastructure and logging to evaluate all flight operations and missions on SITL with reconfigurable tolerances and real-time position tracking.

PROJECTS

Stochastic Computing for Defense Against Hardware Trojan Attacks Fall 2025

- Designed an alternative Roberts edge detection implementation using stochastic computing in SystemVerilog to demonstrate the mitigation of Hardware Trojan effects on stochastic digital circuits.
- Developed gate-level arithmetic modules as well as hardware Trojan triggers/payloads for both our stochastic implementation and an equivalent binary architecture for comparison in image processing.

Result: Built a full simulation workflow that verified the increased accuracy and PSNR for the Stochastic solution when compared to the binary implementation when placed under the same Trojan attacks.

Freecell Solitaire Game Fall 2024

- Developed a Freecell game simulation in Verilog using 2D arrays for the columns of the tableau, free cells, and home cells, as well as 6-bit binary representations to keep track of suit and rank. Implemented game logic to process one move at each clock cycle given a source and destination and check for win condition as well as legality and compliance with Freecell rules.

Result: Built a testbench that displayed the complete solution for Freecell game 8321 by printing the cards in each pile for every state of the game as well as printing the card that was moved and if the game had been won.

Real-time Optical Flow FPGA Accelerator Winter/Spring 2026

- Designed and implemented a fully pipelined Lucas-Kanade optical flow processor in Verilog with a 7-stage pipeline architecture optimized for one pixel-per-cycle throughput at 100 MHz clock frequency.
- Developed custom pipelined divider module using incremental subtraction algorithm to replace behavioral division operators, enabling FPGA synthesis while maintaining pipeline efficiency.
- Demonstrated the design's capability to process 640x480 video frames with continuous pixel streaming for real-time FPGA applications and validated correctness against a reference software implementation.

EDUCATION

Case Western Reserve University Student-Athlete Expected Graduation: May 2026

CLEVELAND, OH - PURSUING BSE IN COMPUTER ENGINEERING, GPA 3.7, DEAN'S LIST

- **Notable Coursework:** FPGAs, Digital Systems Design, VLSI/CAD, Embedded Systems, Logic Design, Data Structures and Algorithms, Artificial Intelligence, Computer Architecture, Database Systems Design
- 4-year starter on Varsity Men's soccer team. All Conference (2025), Academic All District (2024,2025)